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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,392	DYBSETTER ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated October 30, 2006. At this point, no claims have been amended and no claims have been cancelled. There are 42 claims pending in the application; there are 3 independent claims and 39 dependent claims, all of which are ready for examination by the examiner.

I. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-6 and 9-33** are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) in view of Tzeng et al. (US 5,893,153).

3. As per **claims 1, 6, 9, 14, 20-22 and 28-30**, Fadavi-Ardekani discloses

"In a system/system/controller that includes"

"a system memory," as **["memory 200" (Figure 1)]**

"and a plurality of processors" **[With respect to this limitation, Fadavi-Ardekani discloses a plurality of agents that access memory "agents 100-104" (Figure 1) and "agents 100-108" (Figure 2) and explains that "each of the plurality of agents 100, 104 may be any suitable**

processing element, e.g., a digital signal processor (DSP), on demand transfer (ODT) engine, microprocessor or microcontroller" (Column 3, lines 46-49)]

"and one or more other memory consumers that each access the system memory through a memory controller," **[With respect to this limitation, Fadavi-Ardekani discloses a plurality of agents that access memory "agents 100-104" (Figure 1) and "agents 100-108" (Figure 2) and explains that one of the agents can be a master process and "the other agents can be slave peripheral devices or co-processors" (Column 3, lines 50-52)]**

"a method for the memory controller to manage access to the system memory for each of the plurality of processors and the one or more other memory consumers, the method comprising the following:" as **[Fadavi-Ardekani discloses this limitation as "arbiter 102" and explains that "an arbiter and switch 102 allows one of the plurality of agents 100 or 104 o access the shared synchronous memory 200 at any one time" (Column 3, lines 53-55)]**

"an act of the memory controller allotting a first division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a first processor of the plurality of processors such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles;" **[Fadavi-Ardekani discloses this concept as "one of the plurality of agents, e.g., agent 100 may be designated as having a higher level (i.e., a super level) with respect to the other agents, e.g. agents 104 to 108" (Column 5, lines 13-16 and Figures 1 and 2) and explains that the "super agent" is not required to arbitrate for access to memory with the other agents (Column 5, lines 30-38); therefore, the "super agent" is guaranteed access to memory during a first cycle wherein "if a cycle extension of a memory request from the super agent A lasts for N cycles, the first**

cycle might be used by the super agent A to access the shared synchronous memory" (Column 7, lines 7-10 and Figures 2 and 4)]

"and an act of the memory controller allotting a second division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a second processor of the plurality of processors such that memory access is conditionally granted to the second processor during the second division of each of the plurality of memory access cycles"

[Fadavi-Ardekani discloses this concept as "non-super agents arbitrate for ownership and access to the shared synchronous memory 200 during open windows of time, either between accesses by a super agent or the interim during an extended access by the super agent A" (Column 6, lines 60-64) and provides an example in which "if a cycle extension of a memory request from the super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13). It is also taught that "non-super agents" arbitrate for access to memory on a "first-come, first-served bases, on a priority basis, or other suitable decisive decision criteria by the arbiter and switch 202. For instance, the winning non-super agent may be provided time division multiplexed access to the shared synchronous memory" (Column 6, lines 1-8) wherein agents can be processors or other peripheral devices (Column 3, lines 49-52); therefore, processors and peripheral devices arbitrate/compete for memory access during a second memory access cycle, and access might be granted to a processor on a conditional basis].

Fadavi-Ardekani does not disclose expressly that during the arbitration cycle, a processor is given access to memory "subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory."

Tzeng discloses the concept of during an arbitration cycle, giving access to memory to a processor "subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" as **["when an instruction from the core logic unit and a DMA request from an external input/output unit are simultaneously present at the external cache controller, the integrated input/output system maintains data coherency by implementing a rule of procedure that prioritizes the DMA request over the core logic unit instruction" (Column 2, lines 37-42); therefore, when there are not I/O unit requests to access memory, access by the processor/logic unit/cpu will be imposed (*as claimed by Applicant in claim 6*); otherwise, I/O units (*other memory consumers*) will be allowed to access memory (*as claimed by Applicant in claim 9*)]**; therefore, a memory consumer is allowed to access memory during "regardless of having received the request from the second processor to access the system memory during the second division of the second memory access cycle" as (*as in claim 14*) **[DMA accesses are prioritized (Column 2, lines 37-42)]**.

Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access control method/system; which during a second memory access cycle, arbitrates access to memory by multiple agents which may be processors or other

peripheral devices based on priority as taught by Fadavi-Ardekani and further give higher priority to peripheral or I/O devices over processors or core logic units as taught by Tzeng.

The motivation for doing so would have been because Tzeng discloses that during an arbitration cycle, access to memory to a processor should be given "subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" because **["Many external I/O devices operate in real time. Moving DMA instructions ahead of instructions from the core logic unit has the added benefit of ensuring that the external I/O devices properly operate in such a real time environment" (Column 2, lines 53-57)]**.

Therefore, it would have been obvious to combine Tzeng et al. (US 5,893,153) with Fadavi-Ardekani et al. (US 6,401,176) for the benefit of creating a method of controlling memory accesses by multiple units to obtain the invention as specified in claims 1, 20-22 and 28-30.

4. As per **claims 2-5 and 10-13**, the combination of Fadavi-Ardekani and Tzeng discloses "A method in accordance with claims 1 and 9," **[See rejection to claims 1 and 9 above]** "wherein the first division in a given memory access cycle of the plurality of memory access cycles is before/after/adjacent in time/separated in time with the second division in the given memory access cycle" **[Fadavi-Ardekani discloses these limitations as memory access to a super agent (*first processor, as claimed by Applicant*) is given without having to arbitrate with non-super agents (*second processors or other memory customers devices as claimed by applicant*) (Column 5, lines 35-38) wherein "non-super agents" arbitrate for memory access during open windows; for example, "if a cycle extension of a memory request from the**

super agent A lasts for N cycles, the first cycle might by used by the super agent A to access the shared synchronous memory 200, while an open window having a length of N-1 cycles of the free-running clock would be generated for use by the non-super agents, e.g., non-super agent B" (Figures 2 and 4 and Column 7, lines 7-13). Fadavi-Ardekani also discloses; "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67); therefore, a super-agent memory access cycle *(or first cycle, as claimed by Applicant)* may be before/after/adjacent in time/separated in time from a memory access by a non-super agent (*second processors or other memory customers devices as claimed by applicant*)].

5. As per **claims 15, 23 and 31**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system/controller in accordance with claims 1, 20 and 28," **[See rejection to claims 1, 20 and 28 above]** "further comprising the following:"

"an act of the memory controller allotting a third division of each of a plurality of memory access cycles to time-division multiple access of the system memory for a third processor of the plurality of processors such that memory access is guaranteed for the third processor during the third division of each of the plurality of memory access cycles" **[This claim is rejected for the same reasons as noted above for the rejection to claim 1. Additionally, Fadavi-Ardekani discloses that "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67) and explains that one or more super agents might exist (Column 6, lines 66-67);**

therefore, super-agent memory access cycles can occur at any time with higher/guaranteed priority].

6. As per **claims 16-17, 24-25 and 32-33**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system/controller in accordance with claims 1, 15, 20, 23, 28 and 31" **[See rejection to claims 1, 15, 20, 23, 28 and 31 above]** "further comprising the following:" "an act of the memory controller allotting a fourth division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a fourth processor of the plurality of processors such that memory access is conditionally granted to the fourth processor during the fourth division of each of the plurality of memory access cycles subject to a determination that at least one of the one or more other memory consumers has not also requested access to the system memory" **[This claim is rejected for the same reasons as noted above for the rejection to claim 1. Additionally, Fadavi-Ardekani discloses that "super agent A is provided transparent access to the shared synchronous memory 200, i.e., whenever desired. Thus, the super agent A is provided access to the shared synchronous memory 200 without arbitration and/or negotiation" (Column 5, lines 63-67) and explains that one or more super agents might exist (Column 6, lines 66-67); therefore, super-agent memory access cycles can occur at any time with higher/guaranteed priority]**.

7. As per **claims 18 and 26**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system in accordance with claims 1 and 20," **[See rejection to claims 1 and 20 above]** "wherein at least one of the one or more other memory consumers includes a serial interface" **[With respect to this limitation, Fadavi-Ardekani discloses "agents can be slave peripheral devices" (Column 3, lines 51-52 and Figure 2). Tzeng also discloses (*memory consumers as*

claimed by Applicant) **as "I/O devices 54, 55" (Figure 2). These peripheral or I/O devices might be modem, keyboard or serial printers, which are well known serial devices]**.

8. As per **claims 19 and 27**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system in accordance with claims 1 and 20," **[See rejection to claims 1 and 20 above]** "wherein the one or more memory consumers comprise a plurality of memory consumers" **[With respect to this limitation, Fadavi-Ardekani discloses multiple agents accessing memory and explains that "agents can be slave peripheral devices" (Column 3, lines 51-52 and Figure 2). Tzeng also discloses "I/O devices 54, 55" (Figure 2)]**.

9. **Claims 7-8** are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 6 above, and further in view of Chin et al. (US 6,275,885).

10. As per **claims 7-8**, the combination of Fadavi-Ardekani and Tzeng discloses "A method/system in accordance with claim 6," **[See rejection to claim 6 above]** but does not disclose expressly that "the act determining that at least one of the one or more other memory consumers has not also requested access to the system memory during the second division of the first memory access cycle comprises the following:" a request "is not issued by the second processor if the at least one of the one or more memory consumers had requested access" or "request from the second processor is not received by the memory controller if the at least one of the one or more memory consumers had requested access."

Chin discloses a memory access control method/system in which "a request is not issued by the second processor if the at least one of the one or more memory consumers had requested access" or "the request from the second processor is not received by the memory controller if the

at least one of the one or more memory consumers had requested access" as [**"a bus interface unit includes a memory arbiter which grants ownership of the memory bus to a peripheral device cycle rather than a concurrent CPU cycle when certain conditions exist. The bus interface unit therefore involves a mechanism for stalling CPU cycles on the CPU bus until after the peripheral device obtains mastership of the memory bus. In this fashion, the memory arbiter will grant mastership to a peripheral cycle since a CPU derived cycle is prevented from reaching the memory arbiter" (Column 3, lines 7-17) and explains that "upon receiving the priority bus request signal form the bus interface unit, each and every CPU linked to the CPU bus is stalled from sending address and data across the CPU bus" (Column 3, lines 29-32) wherein "by asserting a signal (BNR#) any agent can prevent the current CPU bus owner from issuing new transactions" (Column 9, lines 38-41)**].

Fadavi-Ardekani et al. (US 6,401,176), Tzeng et al. (US 5,893,153) and Chin et al. (US 6,275,885) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access control method/system; which during a second memory access cycle, arbitrates access to memory by multiple agents which may be processors or other peripheral devices based on priority as taught by Fadavi-Ardekani, give higher priority to peripheral or I/O devices over processors or core logic units as taught by Tzeng and further having stalling CPUs from issuing memory access requests or not receiving memory access request by a memory arbiter as taught by Chin.

The motivation for doing so would have been because Chin discloses that CPUs are stalled from issuing memory access requests or these memory access requests are not received by a memory arbiter to **[keep memory coherent and "assure that peripheral-derived data is written into the system memory before that data is read by the CPU" (Column 2, lines 64-60) as peripheral-derived data processing is time critical or real-time (Tzeng; Column 2, lines 53-57)]**.

Therefore, it would have been obvious to combine Chin et al. (US 6,275,885) with Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) for the benefit of creating a method of controlling memory accesses by multiple units to obtain the invention as specified in claims 7-8.

11. **Claims 34 and 40-42** are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 28 above and further in view of the following:

It is noted that the combination of Fadavi-Ardekani and Tzeng does not disclose a memory controller is implemented in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver. However, the examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the controller as being claimed in claim 30 in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver. A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim form the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)).

12. **Claims 35-39** are rejected under 35 U.S.C. 103(a) as being unpatentable by Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) as applied to claim 34 above and further in view of the following:

The combination of Fadavi-Ardekani and Tzeng does not disclose expressly that a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to apply the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G. Applicant has not disclosed that applying the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with any memory size because the combination Fadavi-Ardekani and Tzeng provides a method/system/controller to control accesses to memory by a plurality of processors and other peripheral or I/O devices, regardless of the size of the memory and Fadavi-Ardekani explains that [**"the principles of the present invention relate equally to all types of synchronous memory" (Column 3, lines 44-45)**].

Therefore, it would have been obvious to one of ordinary skill in this art to modify the combination of Fadavi-Ardekani et al. (US 6,401,176) and Tzeng et al. (US 5,893,153) to obtain the invention as specified in claims 35-39.

II. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

13. Applicant's arguments filed on October 30, 2006 with respect to claims **1-42** have been considered but they are not persuasive.

14. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

III. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

15. Claims must be given the broadest reasonable interpretation during examination and limitations appearing in the specification but not recited in the claim are not read into the claim (See M.P.E.P. 2111 [R-1]).

1ST POINT OF ARGUMENT

16. Regarding Applicant's remark that Fadavi-Ardekani does not teach a "memory controller" that is configured to perform an act of "allotting a first division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a first processor such that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles" as Fadavi-Ardekani's disclosed arbiter does not guarantee a first division to a "super agent" because the "super agent" is not required to arbitrate for access; it is the Examiner's position that Fadavi-Ardekani discloses this limitation as **["With higher priority, the super agent is given access to the shared synchronous memory whenever requested and can thus access the shared synchronous memory without halting its operation" (Col. 8, lines 49-57) wherein "a priority level can be assigned to each of the agents 100 to 108 using a hardwired encoder 190 in the arbiter 102a " (Col. 4, lines 45-48);**

therefore, the arbiter is used to encode a priority level to an agent, making this agent a "super agent" such that "memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles" as claimed by Applicant].

17. Furthermore, Fadavi-Ardekani teaches an embodiment in which [**"a non-preemptive locking mechanism to allow an agent to efficiently access the shared synchronous memory by another agent without interruption and/or without affecting the previous agent's access to the shared synchronous memory" (Col. 10, lines 40-44) wherein "pre-arbiter 920... provides ability for any agent to lock its ownership of the shared synchronous memory 200a as necessary. Not all agents need have the ability to lock ownership of the shred synchronous memory 200a... a requesting locking agent is allowed to take advantage of the brief periods (i.e., cycles) of inactivity in the memory access request signal from the currently owning agent. Accordingly, locked ownership of the shared synchronous memory can be determined at a pre-arbitration level... the pre-arbiter 920 may suppress one or more subsequent memory access request signals from any or all non-locking agents or agents not provided with the ability lock ownership, to provide a locked access to the winning locking agent. When the locking signal from the winning locking agent to the pre-arbiter 920 is terminated, the arbiter 102a may be allowed to arbitrate ownership of the shared synchronous memory 200a based, e.g., on a priority established in the priority encoder 190" (Figure 9 and related text)**], therefore, disclosing a "memory controller" that is configured to perform an act of "allotting a first division of each of the plurality of memory access cycles to time-division multiple access of the system memory for a first processor such

that memory access is guaranteed for the first processor during the first division of each of the plurality of memory access cycles" as claimed by Applicant.

2ND POINT OF ARGUMENT

18. Regarding Applicant's remark that Fadavi-Ardekani does not teach "a system memory... a plurality of processors... that each access the system memory through the memory controller" as "super agent" accesses the memory via "communication path 220," Examiner refers Applicant's attention to an embodiment taught by Fadavi-Ardekani in which [**"a non-preemptive locking mechanism to allow an agent to efficiently access the shared synchronous memory by another agent without interruption and/or without affecting the previous agent's access to the shared synchronous memory" (Col. 10, lines 40-44) wherein "pre-arbiter 920... provides ability for any agent to lock its ownership of the shared synchronous memory 200a as necessary. Not all agents need have the ability to lock ownership of the shred synchronous memory 200a... a requesting locking agent is allowed to take advantage of the brief periods (i.e., cycles) of inactivity in the memory access request signal from the currently owning agent. Accordingly, locked ownership of the shared synchronous memory can be determined at a pre-arbitration level... the pre-arbiter 920 may suppress one or more subsequent memory access request signals from any or all non-locking agents or agents not provided with the ability lock ownership, to provide a locked access to the winning locking agent. When the locking signal from the winning locking agent to the pre-arbiter 920 is terminated, the arbiter 102a may be allowed to arbitrate ownership of the shared synchronous memory 200a based, e.g., on a priority established in the priority encoder 190" (Figure 9 and related text)**]. Therefore, Fadavi-

Ardekani discloses "a system memory... a plurality of processors... that each access the system memory through the memory controller" as claimed by Applicant.

3RD POINT OF ARGUMENT

19. Regarding Applicant's remark that the Examiner is relying on personal knowledge as a basis for rejecting claims 34-42 and has not identified any reference of materials as being obvious to combined with the teachings of the cited references as Examiner states "that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the controller as being claimed in claim 28 in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver;" Applicant should note that the Examiner has relied upon (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)) which states that a recitation directed to the manner in which a claim is intended to be used does not distinguish the claim form the prior art if prior art has the capability to do so. Therefore, According to (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987)), the "memory controller... operated in a system that includes a system memory" of claim 28 may be used in a laser transmitter/receiver wherein the laser transmitter/receiver might be a XFP laser transceiver, SFP laser transceiver or a SFF laser transceiver or in any other device in which a "memory controller... operated in a system that includes a system memory" performs the functionality as claimed in claims 28.

4TH POINT OF ARGUMENT

20. Regarding Applicant's remark that the Examiner is relying on personal knowledge as a basis for rejecting claims 34-42 and has not identified any reference of materials as being obvious to combined with the teachings of the cited references as Examiner states that "at the

time the invention was made, it would have been obvious to a person of ordinary skill in the art to apply the controller of claim 30 to a laser transmitter/receiver of 1 G, 2 G, 4 G, 10 G, or greater that 10 G;" Applicant should note that such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose,* 105 USPQ 237 (CCPA 1955).

21. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated October 30, 2006.

IV. CLOSING COMMENTS

Examiner's Note

22. Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing data of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of the final action.

V. STATUS OF CLAIMS IN THE APPLICATION

24. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

25. Per the instant office action, **claims 1-42** have received a second action on the merits and are subject of a final rejection.

26. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VI. DIRECTION OF ALL FUTURE REMARKS

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

28. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

29. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 4, 2007

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100